WHAT IS CLAIMED IS:

1. A semiconductor memory system comprising:

a memory controller;

N system data buses connected to the memory controller, each of the *N* system data buses having a width of *M*/*N* bits, where *M* is a natural number and *N* is a natural number of at least 2; and

first through *P*-th memory module groups, each of the first through *P*-th memory module groups having *N* memory modules, where *P* is a natural number;

wherein the *N* memory modules within each of the first through *P*-th memory module groups are connected to a respectively different one of the *N* system data buses, and wherein the first through *P*-th memory module groups are operated in response to respective first through *P*-th chip select signals.

2. The system of claim 1, wherein *M* is a bit-width of an entire system data bus of the semiconductor memory system.

3. The system of claim 1, wherein the *N* system data buses are wired such that data transmission times are the same from the *N* memory modules within each of the first through *P*-th module groups to the memory controller.

4. The system of claim 1, wherein each of the *N* memory modules includes *L* memory devices, wherein each of the *L* memory devices is divided into *N* banks, and wherein the *N* banks of each of the *L* memory devices share a data bus of *M*/*N* bits and are separately operated in response to the first through *P*-th chip select signals.

5. The system of claim 4, wherein the first through *P*-th chip select signals are respectively applied to the *N* banks.

6. The system of claim 4, wherein each of the *L* memory devices has a data bus width of *M*/*L* bits.

7. The system of claim 1, wherein each of the *N* memory modules includes *L* memory devices, and wherein each of the *L* memory devices has a bus width of *M*/(*N***L*) bits.

8. A semiconductor memory system comprising:

a memory controller;

N system data buses connected to the memory controller, each of the *N* system data buses having a width of *M*/*N* bits, where *M* is a natural number and *N* is a natural number of at least 2;

a first memory module group having *N* memory modules respectively connected to the *N* system data buses, wherein the *N* memory modules of the first memory module group each have a data bus width of *M*/*N* bits and are operated in response to first chip select signals; and

a second memory module group having at least one memory module connected to all of the *N* system data buses, wherein the at least one memory module of the second memory module group has a data bus width of M bits and is operated in response to a second chip select signal.

9. The system of claim 8, wherein *M* is a bit-width of an entire system data bus of the semiconductor memory system.

10. The system of claim 8, wherein the *N* system data buses are wired such that data transmission times are the same from the memory modules of the first memory module group to the memory controller.

11. The system of claim 8, wherein each of the memory modules of the first memory module group includes *L* memory devices, wherein the *L* memory devices are divided into *N* banks, wherein the *N* banks of each of the *L* memory devices share a data bus of *M*/*N* bits and are separately operated in response to the first chip select signals.

12. The system of claim 11, wherein the first chip select signals are respectively applied to the *N* banks.

13. The system of claim 11, wherein each of the *L* memory devices has a data bus width of *M*/*L* bits.

14. The system of claim 8, wherein each of the memory modules includes *L* memory devices, and each of the *L* memory devices has a bus width of *M*/(*N***L*) bits.

15. A semiconductor memory system, the system comprising:

a memory controller;

N system data buses connected to the memory controller, each of the *N* system data buses including a plurality of data buffers and having a width of *M*/*N* bits, where *M* is a natural number and *N* is a natural number of at least 2; and

first through *P*-th memory module groups connected to the *N* system data buses, each of the first through *P*-th memory module groups having *N* memory modules;

wherein the *N* memory modules within each of the first through *P*-th memory module groups are connected to the data buffers of respectively different ones of the *N* system data buses, wherein the first through *P*-th memory module groups are operated in response to respective first through *P*-th chip select signals.

16. The system of claim 15, wherein *M* is a bit-width of an entire system data bus of the semiconductor memory system.

17. The system of claim 15, wherein, for each of the first through *P*-th module groups, the *N* system data buses are wired such that data transmission times are the same from the *N* memory modules within each of the first through *P*-th module groups to the memory controller.

18. The system of claim 15, The system of claim 8, wherein each of the memory modules of the first memory module group includes *L* memory devices, wherein the *L* memory devices are divided into *N* banks, wherein the *N* banks of each of the *L* memory devices share a data bus of *M*/*N* bits and are separately operated in response to chip select signals.

19. The system of claim 18, wherein the chip select signals are respectively applied to the *N* banks.

20. The system of claim 18, wherein each of the *L* memory devices has a data bus width of *M*/*L* bits.

21. The system of claim 15, wherein each of the memory modules includes *L* memory devices, and each of the *L* memory devices has a bus width of *M*/(*N***L*) bits.